Attorney Docket No.
LAM2P258

PATENT APPLICATION

IMPROVED SELF-ALIGNED CONTACT PROCESS IMPLEMENTING BIAS COMPENSATION ETCH ENDPOINT DETECTION AND METHODS FOR IMPLEMENTING THE SAME

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BACKGROUND OF THE INVENTION

Field of the Invention

[1] The present invention relates generally to the fabrication of semiconductor devices and, more particularly, to improving the fabrication sequence in self-aligned contact processes by enhancing the etch endpoint detection of a desired layer.

Description of the Related Art

[2] As is well known, in semiconductor manufacturing, different processes can be implemented to fabricate millions of transistors on a semiconductor chip. An exemplary process is a self-aligned contact (SAC) process, which traditionally is implemented in several stages. First, in the silicon nitride (SiN_3) spacer etch process stage, a silicon nitride layer is deposited on a surface of substrate having fabricated transistors. As is well known, each transistor includes source/drain diffusion regions, a conductive polysilicon gate, and a dielectric gate oxide. This silicon nitride layer is subsequently etched utilizing a plasma etch process, thereby creating silicon nitride spacers alongside the polysilicon gates. Second, in the stop layer cap deposit process stage, a stop layer (e.g., silicon nitride) is deposited over the gate oxides as well as the

source/drain diffusion regions. Next, the interlevel dielectric layer (ILD) is formed in the ILD oxide deposit process stage through successive depositions of a high density plasma (HDP) oxide layer, a tetraethylorthosilicate (TEOS) deposition layer, and an oxide deposition layer (e.g., silicon dioxide).

[3] Next, in the contact lithography process stage, the surface of the ILD layer is patterned using the photoresist mask defining unprotected contact-like portions. Then, in the ILD oxide etch process stage, exposed portions of the ILD layer are selectively removed during an etching process implementing a first set of chemicals. Thereafter, the etching process is repeated in the following stop layer liner etch process stage, wherein the exposed portions of the stop layer (typically, made out of silicon nitride) are removed implementing a second set of chemicals. As is well known, implementing two different sets of chemicals to etch the exposed portions of the ILD oxide layer and silicon nitride stop layer is important, as the removal of silicon nitride requires chemicals with higher selectivity.

[4] Generally, SAC ILD oxide etch and SAC silicon nitride stop layer liner etch implement a dry etching method called plasma etching. The plasma etching process is typically performed in a plasma chamber in which strong electrical fields cause high energy gases containing positively charged ions and negatively charged electrons to be accelerated toward the exposed surface areas of the ILD layer and silicon nitride stop layer. In actuality, the exposed portions of the ILD layer and silicon nitride stop layer are physically removed as a result of being bombarded with positive ions. However, etching the exposed portions of the ILD and silicon nitride stop layers must stop once it has been determined that the ILD and silicon nitride stop layers have been etched

through. As a result, it is imperative to implement an endpoint detection method to stop the etching process once the desired layer has been etched through.

[5] Predominantly, either time mode or optical emission spectroscopy is used to detect the etch endpoint of a desired layer. In the time mode, the thickness of the desired layer as well as the etch rate of the material being removed are used to calculate the approximate length of time required to remove the desired layer. However, because the thickness of wafers and layers formed thereon vary, the time mode has proven to be an unreliable and inefficient method for etch endpoint detection. For instance, due to wafer-to-wafer thickness variation, overetching or underetching of the desired layer may occur. By way of example, the former may cause the removal of portions of the underlying silicon substrate layer or polysilicon gate whereas the latter necessitates further work on the wafer so as to remove the remaining exposed portions.

[6] In the alternative optical emission spectroscopy method, the light emitted by the gases within the etch reactant chamber is used to identify the specific material being etched. As the light emission intensity is directly proportional to the concentration of a specific gas within the etch reactant chamber, the endpoint detector can in theory determine when the etching of a desired material has concluded. However, as the changes in the semiconductor substrate fabrication design rules have enabled the fabrication of smaller and smaller semiconductor substrates, the surface area of contacts and vias (i.e., the exposed oxide portions of the ILD layer) have shrunk (for instance, compare a typical contact oxide area which ranges from 2% to .5% to an expected contact oxide area of .2% in the near future). Consequently, the concentration of the material being etched in the plasma has decreased, thus creating a

rather small change in the plasma at etch endpoint. Ultimately, this small change in the plasma results in small changes in the optical emission signal, thus hindering the optical emission endpoint detection process. Additionally, the optical emission endpoint is designed to be monitored through a transparent window defined within etch reactant chamber. However, as the etching process progresses, monitoring optical emission endpoint signal becomes impossible since visibility reduces as etch polymers build up and cover the transparent window over time. As a result, the optical emission endpoint has also proven to be unreliable in etch endpoint detection, as overetching or underetching of the desired layer may occur.

[7] Accordingly, currently, silicon nitride stop layers are being implemented to compensate for the overetching of the underlying layers. However, besides creating a margin for error, silicon nitride stop layers are not required in the fabrication of the semiconductor devices. Thus, the unreliability of the two predominantly implemented etch endpoint detection processes has added two extra fabrications stages to the SAC contact etch processes, unnecessarily increasing the cost associated with SAC contact process while needlessly reducing throughput.

[8] In view of the foregoing, a need exists for a semiconductor fabrication methodology that eliminates extra fabrication stages implemented in a self-aligned contact process thus reducing fabrication cost while increasing wafer throughput.

SUMMARY OF THE INVENTION

[1] Broadly speaking, the present invention fills these needs by providing an apparatus and methodology for optimizing the self-aligned contact processes through eliminating the stop layers, thereby reducing fabrication cost while increasing wafer throughput. Preferably, an interlevel dielectric (ILD) layer of the present invention is formed substantially directly on the substrate and the gate structures without a need to include stop layers as a process margin. In one preferred embodiment, the present invention implements an anticipated ascertained change in a compensation bias voltage of an electrostatic chuck disposed within a reactant etch chamber as evidence of etch endpoint of a desired layer in self-aligned contact (SAC) processes.

[2] It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device, or a method. Several inventive embodiments of the present invention are described below.

[3] In one embodiment, a method for enhancing the fabrication process of a self-aligned contact (SAC) structure is disclosed. The method includes forming a transistor structure on a surface of a substrate. The method also includes forming a dielectric layer directly over the surface of the substrate without forming an etch stop layer on the surface of the substrate. Also included in the method is plasma etching a contact hole through the dielectric layer in a plasma processing chamber. The method also includes monitoring a bias compensation voltage of the plasma processing chamber during the plasma etching process and discontinuing the plasma etching process upon detecting an endpoint signaling change in the bias compensation voltage.

[4] In another embodiment, a method for enhancing the fabrication process of a self-aligned contact (SAC) is disclosed. The method includes forming a transistor structure on a substrate. The transistor structure includes a gate structure formed over a first surface of the substrate. The method further includes forming spacers along sidewalls of the gate structure and forming source/drain diffusion regions into the first surface of substrate. The source/drain diffusion regions are defined substantially outside of the spacers formed along the sidewalls of the gate structure. The method further includes forming an interlevel dielectric (ILD) layer directly over the first surface of the substrate such that the ILD layer overlies the gate structure, the spacers, and the first surface of the substrate without forming a stop layer. The method also includes forming a contact hole and a via hole in the ILD layer implementing a plasma etching process. As designed, the contact hole is defined to a top layer of the gate structure and the via hole is defined to the source/drain diffusion regions. Further included in the method are monitoring a bias compensation voltage during the plasma etching process and discontinuing the plasma etching process when an endpoint signaling change in the bias compensation voltage is detected.

[5] In still another embodiment, a bias compensation self-aligned contact (SAC) etch endpoint detecting system is disclosed. The system includes an etch reactant chamber, an ESC power supply, and a signal processing computer. The etch reactant chamber is configured to include an electrostatic chuck (ESC) designed to support a substrate having an ILD layer to be etched, a top electrode, and a bottom electrode. The ESC power supply is coupled to the ESC and is configured to function as a bias compensating power supply. The signal processing computer is configured to monitor a bias compensation signal generated by the ESC power supply. The etch process is

carried out in the etch reactant chamber and is configured to be discontinued when the bias compensation signal is determined to have a previously ascertained characteristic evidencing an etch endpoint of the ILD layer.

[6] In yet another embodiment, a method for accurately detecting a plasma etch endpoint of a self-aligned contact (SAC) is disclosed. The method includes providing a substrate having a transistor structure on a surface of the substrate. Also included in the method is forming a dielectric layer directly over the surface of the substrate without forming an etch stop layer thereon. The method further includes inserting the substrate into a plasma etching chamber so as to plasma etch a contact hole into the dielectric layer. Also included are introducing etchant gases into the plasma etching chamber and powering up the plasma etching chamber. The powering up of the plasma etching chamber is configured to strike a plasma so as to commence the plasma etching process. The method also includes monitoring a bias level of the plasma etching chamber during the plasma etching process and discontinuing the plasma etching process when an endpoint signaling change in the bias compensation voltage is detected.

[7] The advantages of the present invention are numerous. Most notably, bias compensation self-aligned contact etch process of the present invention eliminates unnecessary fabrication stages associated with the stop layers, thus reducing the fabrication cost. Additionally, as the bias compensation SAC contact etch process of the present invention can accurately control the etch process, the SAC contact etch process of the present invention can be stopped once the underlying source/drain regions or polysilicon gates are exposed. Thus, the bias compensation SAC etch process of the present invention can be used to repeatedly and accurately detect etch

endpoint in wafers having different thickness. Yet another advantage is that the bias compensation SAC process of the present invention implements an ascertained anticipated change in the bias compensation voltage as evidence of etch endpoint. Yet another advantage is that as the bias compensation SAC etch process of the present invention implements changes in the resistive properties of the wafer. This is in contrast to the time mode and optical emission methods which respectively implement the time and removal rate of a specific material or changes in the plasma to detect the etch endpoint. In this manner, the embodiments of the present invention eliminate the shortcomings associated with the time mode and optical emission spectroscopy etch endpoint detection methods.

[8] Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[1] The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, and like reference numerals designate like structural elements.

[2] Figures 1A-1C depict the different stages of fabricating a wafer implementing a self-aligned contact (SAC) process, in accordance with one embodiment of the present invention.

[3] Figure 2 is a schematic and simplified illustration of an exemplary bias compensated bi-polar ESC etch system, in accordance with another embodiment of the present invention.

[4] Figure 3A is a schematic and simplified illustration of an exemplary bias compensation etch system, in accordance with yet another embodiment of the present invention.

[5] Figure 3B is a simplified schematic illustration of the creation of an electrical path between a plasma and the wafer in the exemplary bias compensation etch system depicted in Figure 3A, in accordance with still another embodiment of the present invention

[6] Figure 4 illustrates a graph plotting bias compensation voltage of the ESC vs. etch time, in accordance with still another embodiment of the present invention.

[7] Figure 5A is a flowchart diagram illustrating method operations performed in an exemplary bias compensation etch system, in accordance with yet another embodiment of the present invention.

[8] Figure 5B is a flowchart diagram illustrating the introduction of etchant gases into a chamber, in accordance with still another embodiment of the present invention.

[9] Figure 5C is a flow chart diagram illustrating the method operations performed in the powering up a chamber, in accordance with yet another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[1] An invention for increasing wafer throughput while minimizing costs incurred in fabricating self-aligned contact processes through eliminating stop layers, is disclosed. Preferably, the present invention implements an expected ascertained change in a compensation bias voltage of an electrostatic chuck disposed within a reactant etch chamber as evidence of etch endpoint in a self-aligned contact process. In one embodiment, the present invention correlates a step increase in a bias compensation voltage of an electrostatic chuck disposed within an etch reactant chamber with the length of time required to physically remove an interlevel dielectric layer (ILD) layer before exposing the underlying source/drain diffusion regions or gate structures.

[2] Figures 1A-1C depict the different stages of fabricating a wafer 100 implementing a self-aligned contact (SAC) process, in accordance with one embodiment of the present invention. As shown, the embodiment of Figure 1A depicts a substrate 102 subsequent to the fabrication of spacers 110. The substrate 102 has a plurality of transistors, each of which includes source/drain diffusion regions 106, a conductor polysilicon gate 108, a dielectric gate oxide 112, and spacers 110. Typically, in the SAC process, the spacers 110 are made out of silicon nitride and are formed alongside the polysilicon gates 108 and gate oxides 112. For instance, in the first process stage, the spacers 110 are formed through depositing a silicon nitride layer on the surface of the substrate 102 and polysilicon gates 108, and subsequently etching the same by using a plasma etching process. Also included in the illustrated substrate 102 are shallow trench isolation regions (STIs) 104.

[3] Following the formation of the spacers 110, impurities are implanted into the source/drain diffusion regions 106 of the substrate 103 outside of the polysilicon gates 108, gate oxides 112, and the spacers 110. Once implanted, a heat treatment is performed so as to activate the impurities implanted within the source/drain diffusion regions 106. Thereafter, in the second process stage depicted in the embodiment of Figure 1B, an interlevel dielectric layer (ILD) 119 is formed over the substrate 102. As shown, the ILD layer 119 is created through consecutive deposition of an oxide layer 114 using the high-density plasma chemical vapor deposition (HDPCVD) technique, a tetraethylorthosilicate (TEOS) layer 116, and an oxide layer 118. Of course, any suitable oxide formation process may be used.

[4] Next referring to Figure 1C, the third and fourth stages of the SAC process of the present invention can further be understood. In the contact lithography process stage (i.e., the third process stage), a photoresist mask 121 is used to pattern the ILD layer 119 defining unprotected and exposed contact/via-like portions thereon. Subsequently, in the SAC oxide etch process stage (i.e., fourth process stage), the exposed portions of the ILD layer 119 are selectively removed in a plasma etching process implementing a set of chemicals. In this manner, a plurality of contact holes 120 and via holes 122 are formed within the ILD layer 119, which once filled with a conductive material will provide electrical connection between the successive conductive layers.

[5] As will be discussed in more detail below, the present invention eliminates the silicon nitride stop layers by implementing bias compensation etch endpoint detection. Consequently, the SAC process of the present invention employs two process stages less than the conventional SAC processes. Specifically, the present invention

eliminates the silicon nitride cap deposition and SAC silicon nitride liner etch, as the bias compensation endpoint detection provides such accuracy, which renders using stop layers as process margins redundant. As a consequence, the present invention reduces fabrication cost incurred in SAC processes while it increases wafer throughput.

[6] Figure 2 is a schematic and simplified illustration of an exemplary bias compensated bi-polar ESC etch system 200, in accordance with one embodiment of the present invention. The bias compensated bi-polar ESC etch system 200 includes an etch reactant chamber 204, a bi-polar ESC 206, a radio frequency (RF) power supply 208, an ESC power supply 209, and a signal processing computer 212. The bi-polar ESC 206 includes a pair of conductive portions, poles 206a and 206b configured to function as a pair of electrodes. The pole 206a is coupled to a positive terminal of the ESC power supply 209 and is configured to function as a positive pole. In a like manner, the pole 206b is coupled to a negative terminal of the ESC power supply 209 and is designed to function as the negative pole. A supply tube 307 formed within the ESC chuck 206 is configured to deliver a cooling gas (e.g., helium, etc.) to the wafer 103 during the etch process.

[7] As shown in Figure 2, the RF power supply 208 is coupled to the electrostatic chuck (ESC) 206 and is configured to excite the plasma released into the etch reactant chamber 204. Once activated, the ESC power supply 209, the RF power supply 208, and the plasma released into the etch reactant chamber 204 are configured to induce a positive potential and negative potential on the respective positive pole 206a and negative pole 206b. As a result, electrostatic forces are generated between the positive and negative poles 206a and 206b and their respective overlaying regions of the wafer

103. In this manner, the generated electrostatic forces securely hold the wafer 103 in place with respect to the ESC 206 during the etching process.

[8] Besides assisting to keep the wafer 103 in place with respect to the ESC 206, the ESC power supply 209 further functions as a bias compensating high-voltage supply that powers the ESC 206. As used herein, "bias compensation" is defined as a method used to regulate the voltage present on the wafer 103. As designed, the current from the ESC 206 to the plasma is minimized, thereby ensuring equal clamping force at each of the positive and negative poles 206a and 206b by generating equal electrostatic force between each of the positive and negative poles 206a and 206b and the plasma.

[9] The signal processing computer 212 monitors a bias compensation signal 210 generated by the ESC power supply 209 in real time. As designed, the bias compensation signal 210 is configured to be sensitive to any change in the resistance of the wafer 103. As will be discussed in more detail with respect to Figures 3A-3B and 4, the embodiments of the present invention implement an endpoint signaling change. That is, the embodiments of the present invention implement a previously ascertained step increase (e.g., change) in the bias compensation signal 210 generated by the ESC power supply 209 to detect the etch endpoint.

[10] An ascertained change in the bias compensation voltage of an ESC 306 due to the creation of an electrical path between a plasma 322 and the wafer 103 can further be understood with respect to an exemplary bias compensation etch system 300 depicted in Figure 3A, in accordance with one embodiment of the present invention. The bias compensation etch system 300 includes an etch reactant chamber 304, RF power components 308 and 318, and an endpoint monitoring circuitry 312. As

illustrated in the embodiment of Figure 3A, the RF power component 318 is coupled to the shower head 316 and is configured to excite the plasma 320 from the above while the RF power component 308 is coupled to the ESC 306 so as to excite the plasma 320 from below. As shown, the RF power components 318 and 308 are grounded.

[11] Disposed within the etch reactant chamber 304 are the showerhead 316, a plurality of containment rings 324, the ESC 306, and a wafer 103. The plasma 320 is created in a plasma region 322 disposed within the etch reactant chamber 304, and process gasses are passed through the showerhead 316 having a plurality of holes 316a. The containment rings 322 are configured to substantially confine the plasma 320 within the plasma region 322. The wafer 103 is disposed over the ESC 306 and may be any suitable semiconductor wafer or substrate. A plurality of exhaust pipes 328a and 328b are disposed outside of the etch reactant chamber 304 to release the contents of the reactant etching chamber 304 (e.g., plasma 320, by-products, polymers, etc.)

[12] The ESC 306 depicted in this example is a bi-polar ESC and is configured to have a pair of electrodes 306a and 306b, respectively, coupled to a positive and negative terminals of the endpoint monitoring circuitry 312. The ESC 306 may further include one or more supply tubes 307, which may be fed through one or more portions of the ESC 306 so as to supply a cooling gas. Additionally, one of ordinary skill in the art must appreciate that the ESC poles may assume any configuration.

[13] As described in more detail with respect to Figure 2, the endpoint monitoring circuitry 312 performs several functions. For instance, the endpoint monitoring circuitry 312 functions as a bias compensating power supply that provides power to the

ESC 306. The endpoint monitoring circuitry further generates a bias compensation signal, which reflects the changes in the resistance of the wafer 103. Yet another function of the endpoint monitoring circuitry 312 is to monitor the bias compensation signal, searching for the expected change in the bias compensation, as the etch process approaches the endpoint.

[14] The SAC plasma etch process of the present invention is configured to follow a specific combination of process parameters to etch through the ILD layer (e.g., etch reactant chamber pressure, gas mixtures, gas flow rates, temperature, RF power (top and bottom), wafer position with respect to the plasma, etc.). Preferably, in one implementation, to etch through the ILD layer, the plasma etch process maintains approximately about 82 militorr (mT) pressure inside the etch reactant chamber. The plasma etch process further applies approximately about 1400 watts (W) and 1100 watts (W) through the RF power component 318 and RF power component 308, respectively. Additionally, the chemistry implemented preferably contains argon, C_4F_6, oxygen, each having a flow rate of 260 standard cubic centimeter per minute (sccm), 11 sccms, 12 sccms, respectively. However, it must be appreciated by one having ordinary skill in the art that depending on the type of material being etched, a wide range of gas chemistries may be implemented (e.g., fluorine may be used to etch SiO_2, chlorine may be used to etch aluminum, and chlorine, fluorine, and bromine may be used to etch silicon, oxygen may be used to etch photoresist, etc.).

[15] Reference is now made to Figure 3B depicting a partial, simplified, and magnified portion 311 illustrated in Figure 2B, in accordance with one embodiment of the present invention. As shown, the strong electrical field created within the etch reactant chamber 304 causes the positively charged ions 320' of the plasma 320 to

accelerate toward the photoresist 121 and the exposed portions of the ILD layer 119. In this manner, the positive ions 320' bombard the photoresist 121 and the exposed portions of the ILD layer 119 and gradually remove the exposed portions of the ILD 119.

[16] Initially, due to the ILD layer 119 being a dielectric, the resistance between the ILD layer 119 and the plasma 320 is significantly high. However, as the exposed portions of the ILD layer 119 are gradually etched and a thickness 330 of the exposed portions of the ILD layer 119 decreases, the resistance between the ILD layer 119 and the plasma 320 is reduced. As a result, an electrical path 332 is slowly created from the plasma 320 to the underlying layer, the source/drain diffusion regions 106 of the silicon substrate 102 or the polysilicon gates 112. However, the step rise in the bias compensation voltage occurs when the exposed portions of the ILD layer 119 are etched through, down to the source/drain diffusion regions 106 of the silicon substrate layer 102 (or even the polysilicon gates 112). Thus, the change in the resistance of the wafer 103 ultimately leads to a measurable change in the bias compensation voltage. Thus, any change, whether up or down, which can be differentiated from some constant flow can function as an indicator of reaching end point. In experiments, it has been noticed that the change has varied between about five (5) V and about 30 V. Thus, advantageously, the bias compensation SAC etch system of the present invention has eliminated the need to implement the silicon nitride stop layers typically implemented as process margins in the conventional SAC etch processes.

[17] Figure 4 illustrates a graph 406 that plots bias compensation voltage of the ESC vs. etch time, in accordance with one embodiment of the present invention. As shown, having a bias compensation V-axis 404 as the y-axis and the etch time t-axis 402 as the

x-axis, the graph 406 illustrates the changes in the ESC bias compensation voltage as the ILD layer is etched. At time t_0 412, the bias compensation voltage of the ESC is measured to be about V_a, which corresponds to a point 418 on the bias compensation V-axis 404 and the graph 406. In this example, once etching of the ILD layer is initiated, the graph 406 starts ascending and continues to do so as the etch process continues. Once the etch process approaches the point in time where the desired layer (i.e., the ILD layer) has been removed and the underlying layer (i.e., the source/drain regions of the silicon substrate or the polysiclicon gates) has been exposed (e.g., target endpoint), an endpoint signal in the form of a step increase 406a, is detected in the graph 406. By way of the example depicted in Figure 4, the step increase 406a as defined between points 408 and 410 of the graph 406 may occur between the corresponding time range of t_1 to t_2 and respective anticipated bias compensation voltage range of V_1 to V_2.

[18] At the beginning of the etch process, t_0, the ILD layer provides a substantially higher resistance between the underlying source/drain regions of the substrate silicon and the plasma. This resistance is reduced as the exposed portions of the ILD layer are gradually removed through the etch process. As a result, an electrical path is created from the plasma to the underlying source/drain regions of the silicon substrate. However, the bias compensation voltage is very sensitive to changes in the wafer resistance. Thus, in response to the changes in the wafer resistance, the bias compensation voltage is increased from a bias compensation voltage V_a to V_1, as the etch process continues from t_0 to t_1, creating an ascending graph 406.

[19] Once the exposed portions of the ILD layer are physically removed and the underlying source/drain regions of the silicon substrate are exposed, the etch endpoint

signal in the form of the step increase 406a is detected in the ESC bias compensation voltage. For instance, in one implementation, the point 408 of the graph 406 corresponds to the time t_1 in which at least a portion of the underlying source/drain regions of the silicon substrate become exposed. Comparatively, a point 410 of the graph 406 corresponds to a time t_2 at which the exposed portions of the ILD layer have substantially been removed exposing the underlying source/drain regions of the silicon substrate and the polysilicon gates.

[20] Although in this embodiment the etch process endpoint is evidenced with a step increase in the bias compensation voltage, in a different example, the etch process endpoint may be evidenced by a sharp downward slope, a spike, or a sudden dip in the bias compensation signal. Therefore, it must be appreciated that irrespective of the shape of the bias compensation signal, the end of the etch process is evidenced with a distinct change in the bias compensation voltage. Thus, performing sample etching operations on sample substrates can be used to determine the specific characteristics and shape of the etch endpoint bias compensation signal. In this manner, the endpoint monitoring systems can be instructed to search for the ascertained characteristic and shape in the bias compensation plot so as to define the etch endpoint. Additional details concerning implementing the bias compensation to detect the endpoint of an etch process are described in U.S. Patent No. 6,228,278, issued on May 8, 2001, and entitled "Methods and apparatus for determining an etch endpoint in a plasma processing system," having inventors Jaroslaw W. Winniczek, M. J. Francois Chandrasekar Dassapa, Eric A. Hudson and Mark Wiepking. The disclosure of this U.S. Patent, which is assigned to Lam Research Corporation, the assignee of the subject application, is incorporated herein by reference.

[21] Reference is now made to a flowchart diagram 500 of Figure 5A illustrating method operations performed in a bias compensation SAC etch system of the present invention, in accordance with one embodiment of the present invention. The method begins in operation 502 in which a substrate having an ILD layer to be etched is provided. As was explained in more detail above with reference to Figures 1A-1C, the bias compensation SAC etch system of the present invention can be implemented to detect the etch endpoint in substrates which do not include silicon nitride stop layers. Thus, as discussed above, advantageously, the ILD layer of the present invention is formed substantially directly on the silicon substrate and the polysilicon gates without a need to include stop layers as a process margin.

[22] Next, in operation 504, the substrate is inserted into a chamber and is disposed on an electrostatic chuck (ESC). In addition to the ESC, in one example, the chamber further includes a showerhead, containment rings, and other standard chamber hardware and associated software. Once the substrate is inserted into the chamber, etchant gases are introduced into the chamber in operation 506. In one embodiment, a plurality of holes defined within the showerhead are implemented to introduce the etchant gases into the chamber. Further information with respect to the gases implemented as etchants and their compositions is provided below in connection with Figure 5B.

[23] Continuing to operation 508, the chamber is powered up to strike the plasma, thereby commencing the etching operation. For instance, in one example, once an RF power supply coupled to the ESC is turned on, the gases released into the chamber are excited, initiating the plasma etching process. Additional information with respect to powering up the chamber is provided below in connection with Figure 5C. Once the

etching operation has commenced, in operation 510 a bias level of the substrate is monitored. This is important as the current flowing to the ESC poles change due to the changes in the substrate bias level as the etching operation continues. In one embodiment, these current changes are used to produce a feedback signal to the bias compensation power supply designed to maintain the current flow to the ESC poles substantially equal. Thus, as the etching operation progresses, the changes in the wafer bias level ultimately leads to changes in the bias compensation voltage.

[24] Once a target bias compensation level is reached, the etching process is discontinued in operation 512. Specifically, this occurs when the exposed portions of the ILD layer have substantially been removed thereby exposing a portion of the underlying source/drain regions of the silicon substrate or the polysilicon gates. At this time, in one example, an etch endpoint signal in a form of a step increase can be detected in the bias compensation voltage. In this operation, the etch process is discontinued once the step increase in the bias compensation level is detected.

[25] Finally, in operation 514, the substrate is removed from the chamber and the chamber and the substrate are prepared for further processing, if desired. That is, the chamber is prepared for performing an etch operation on a different substrate.

[26] The introduction of etchant gases into the chamber can further be understood with respect to the flow chart diagram depicted in Figure 5B, in accordance with one embodiment of the present invention. First, in operation 506a an argon level is set. By way of example, the flow rate of argon may be set to be 260 standard cubic centimeter per minute (sccm). Next, in operation 506b a level is set for C_4F_6 which is subsequently followed by operation 506 wherein a level is set for oxygen. For instance, in one preferable example, the flow rate of C_4F_6 and oxygen may be set to be

about 11 sccm, about 12 sccm, respectively. However, one of ordinary skill in the art must bear in mind that depending on the type of material being etched, a wide range of gas chemistries may be implemented.

[27] Reference is made to the flow chart diagram of Figure 5C illustrating the method operations performed in powering up the chamber in operation 508, in accordance with one embodiment of the present invention. In operations 508a and 508b, a top electrode power and a bottom electrode power are set, respectively. As discussed in more detail above with reference to Figure 3A-3B, each of the top and bottom electrodes are coupled to a radio frequency (RF) power. Preferably, in one example, each RF power applies approximately about 1400 watts (W) and 1100 watts (W) to the respective top electrode and bottom electrode. Finally, a pressure level is set in operation 508c, which in one implementation, maintains approximately about 82 militorr (mT) pressure inside the etch chamber.

[28] Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is: